A 23GHz Differential Amplifier with Monolithically Integrated T-Coils in 0.09µm CMOS Technology

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Abstract — **We present a four-stage differential amplifier using coupled inductors in a T-coil configuration to match the capacitive load to the driving transistor. The chip was fabricated in a 90nm CMOS technology [1] and achieves a bandwidth of 23GHz with a differential gain of 18dB at 1.2V supply voltage. At 1.0V supply voltage the circuit displays a bandwidth of 23GHz with 15dB gain at 54mW dissipated power.**

I. Introduction

Modern CMOS technologies will soon be used for data transmission at 40Gbit/s and beyond. For the design of broadband amplifiers, the goal is to maximize gain and bandwidth, while at the same time minimize power consumption. This can be achieved by employing inductive peaking in the amplification stages. Fig. 1 displays three possible implementations of a differential gain cell. While ordinary gain stages with resistive loads (Fig. 1a) achieve a certain bandwidth, this value can in theory be extended by roughly a factor of two through inductive peaking (Fig. 1b), assuming ideal inductors with no losses due to substrate coupling and skin effect. The use of coupled inductors in a "T-coil" configuration (Fig. 1c), however, can further increase the bandwidth [2,3]. In this paper we present an implementation of an amplifier with four gain cells using T-coils, followed by a buffer stage driving a 50Ω load. We show how the coupled inductors of the T-coil can be designed on-chip by tapping a single planar inductor in the middle.

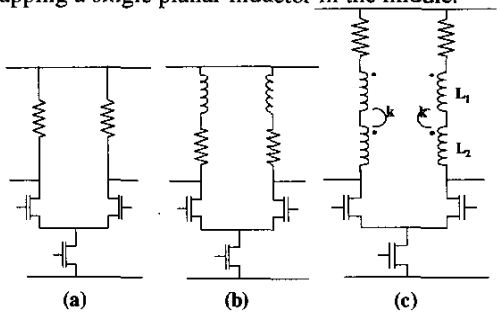

Fig. 1. Differential amplification stages using (a) resistive loads, (b) inductive shunt peaking, (c) T-coil peaking.

II. T-Coil Matching Network

It can be shown that for the T-coil matching network depicted in Fig. 2 the input impedance $Z_1=v_1/i_1$ seen from the current source equals the load R_L for all frequencies if the component parameters are chosen [2] according to

$$L_{1,2} = \frac{R_L^2 C_L}{4}\left[1+\frac{1}{4\zeta^2}\right], \quad k = \frac{4\zeta^2-1}{4\zeta^2+1}, \quad C_c = \frac{C_L}{16\zeta^2}. \tag{1}$$

The transimpedance $Z_2=v_2/i_1$ is then described by a second order transfer function having a pair of complex poles and no zeroes

$$\frac{v_2}{i_1} = \frac{R_L\omega_0^2}{s^2+2\zeta\omega_0 s+\omega_0^2}, \tag{2}$$

whereby the resonance frequency is linked to the damping factor by

$$\omega_0 = 4\zeta/(R_L C_L). \tag{3}$$

Setting $\zeta^2 = ½$ results in a maximally flat (Butterworth type) amplitude response. The –3dB frequency of a single stage is multiplied by a factor of 2.8 compared to purely resistive loads at no power penalty. In addition, due to the complex poles in the transfer function, bandwidth shrinkage caused by cascading the amplifiers is reduced. It can easily be shown that for $\zeta^2 = ½$ the bandwidth of a cascade of n identical stages degrades only with $\sqrt[4]{n}$. In practice, the bandwidth gain of the T-coil configuration is limited however due to the series resistance of L_2 and the degradation of the inductors caused by losses in the substrate and the skin effect.

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II. Circuit Architecture

The amplifier consists of four identical gain stages, followed by a buffer stage as depicted in Fig. 3. The gain stages use the coupled-inductor loads of Fig 1c, while the output buffer uses simple resistive loads with a nominal value of 50 Ω to minimize reflections.

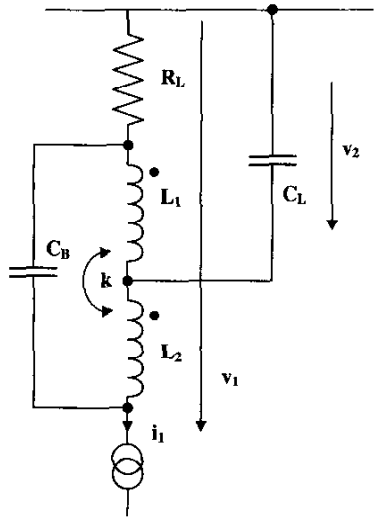

Fig. 2. Schematic of the T-coil network. The load capacitance C_L is the input capacitance of the next amplification stage.

All resistors are implemented as non-salicided poly resistors with offer small parasitic capacitance. PMOS transistors are connected in parallel to the load resistors in order to allow tuning the resistance with an externally supplied voltage. Choosing $\zeta^2 = 1/2$ results in a coupling coefficient k of 1/3, which can easily be achieved with the proposed inductor topology. L_2 was chosen bigger than L_1 in order to compensate for the capacitance on the drain node.

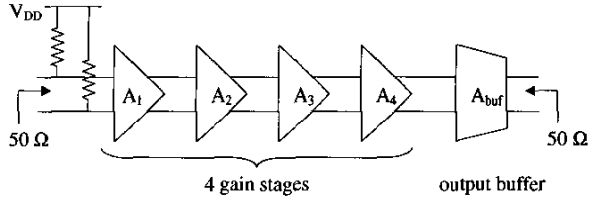

Fig. 3. Block diagram of the amplifier: Four amplification-stages are followed by a 50 Ω buffer stage.

III. Implementation of the T-coils

Monolithically integrated inductors are most frequently used in oscillators, where they require high quality (Q) factors, which mandates minimizing the series resistance. For broadband amplifiers, the series resistance is of lesser importance since it can be absorbed into the load resistance. On the other hand, a small inductor area is required to reduce the capacitive coupling to the substrate, thereby achieving high resonance frequencies. Hence, the width of the inductor wire was chosen as small as possible, limited only by electromigration constraints. The distance between the windings was chosen close to the minimum distance allowed for the used metal layer. Thus, the resulting layout is very compact. Implemented on the top layer of a 6 level metal stack (4 single and 2 double thick metals), the simulated resonance frequency for each L_1 and L_2 was > 70GHz.

Fig. 4 shows the layout of the coupled inductors. In a first iteration, the inductor geometry was found by applying the formulas from [4], which calculate inductance L as a function of the outer diameter d_{out}, the number of turns n, conductor width w and spacing s. To calculate the coupling factor k, first the inductances of L_1 and L_2, and the total inductance L_{tot} are calculated

$$\begin{aligned} L_1 &= L(d_{out}, n_1), \\ L_2 &= L(d_{out} - 2n_1(w+s), n_2), \\ L_{tot} &= L(d_{out}, n_1 + n_2), \end{aligned} \tag{4}$$

where n_1 and n_2 represent the number of turns of the inner and outer conductor, respectively. The coupling factor is then given by

$$k = \frac{L_{tot} - L_1 - L_2}{2\sqrt{L_1 \cdot L_2}}. \tag{5}$$

In a second step, the geometry was then simulated with a field simulator and the resulting S-parameter model used directly in circuit simulations. The actual parameters of the T-coil inductors are summarized in Table 1.

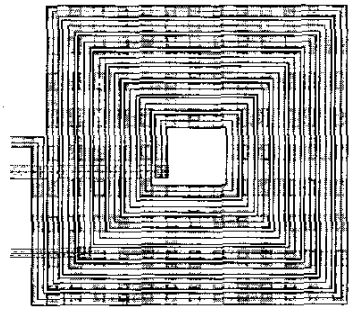

Fig. 4. Layout of the T-coil load. The two coupled inductors are constructed from a single planar inductor, which is tapped in the third turn.

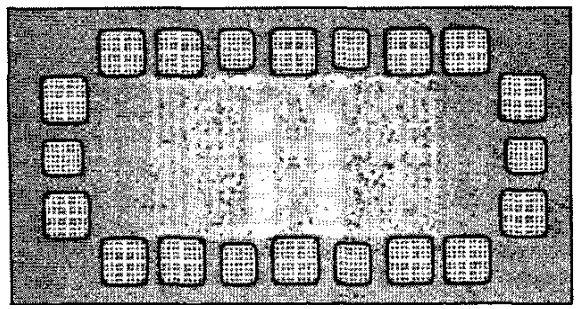

Fig. 5. Photograph of the fabricated amplifier chip. Overall chip dimensions are 1x0.5mm^2. Active area is 170 x 250µm^2.

	Inner Inductor	Outer Inductor
Metal width	1.44 µm	
Spacing	0.36 µm	
Total dimension	24 µm x 24 µm	35 µm x 35 µm
Number of Turns	5	3
Inductance	0.45 nH	0.59 nH
Coupling factor	0.35	

TABLE 1. Summary of electrical and layout parameters of the coupled inductor structure.

IV. Measurement Results

The circuit was tested on-wafer with high-speed power-ground-signal-ground-signal-ground-power (P-G-S-G-S-G-P) probes, and characterized with an HP 8510C vector network analyzer. The measurements were done single-ended, with one input and one output connected to the vector analyzer, the other ports terminated with 50Ω resistors. Bias-T's were used both at the two inputs and outputs to set appropriate common-mode voltage levels.

Measurement results for a supply voltage of V_{DD}=1.2 V are shown in Fig. 6. The DC resistance of the input and output on-chip terminations were measured to be 54 and 57 ohms, respectively, resulting in small input and output reflections. A small-signal single-ended forward gain of 12dB was measured, corresponding to a differential gain of 18dB. The -3dB bandwidth was 23GHz. Power consumption was 67mW for the 4 amplifying stages and 27mW for the output buffer stage. Since the output buffer stage attenuates the signal by 2.5dB, the gain per stage is 5dB.

Operating the chip with a supply voltage of V_{DD}=1.0V resulted in a differential gain of 15dB and a -3dB bandwidth of 23.2GHz, as shown in Fig. 7. Power consumption in the four amplification stages and the buffer stage was 44mW, and 10mW, respectively, including 12mW for biasing and excluding power dissipated in the input termination resistors. These results compare favorably with present implementations of wideband amplifiers in CMOS [5][6], where maximum bandwidth values of 10GHz and 8.5GHz were achieved at gains of 5dB and 5.5dB, respectively.

Fig. 8 shows the single-ended eye diagram for the case of a 20Gbit/s pseudo-random signal and a 56mV p-p input signal. The signal was generated by multiplexing 4 delayed versions of the original 2^{31}-1 pseudo random sequence.

Fig. 9 displays the single-ended data eye for 30Gbit/s and 112mV p-p input signal amplitude. Amplification is smaller in this case since the amplifier was tuned by reducing the load resistance to display a 3dB peaking in order to offset the significant losses of the cables connecting the measurement setup (-3dB at 16GHz).

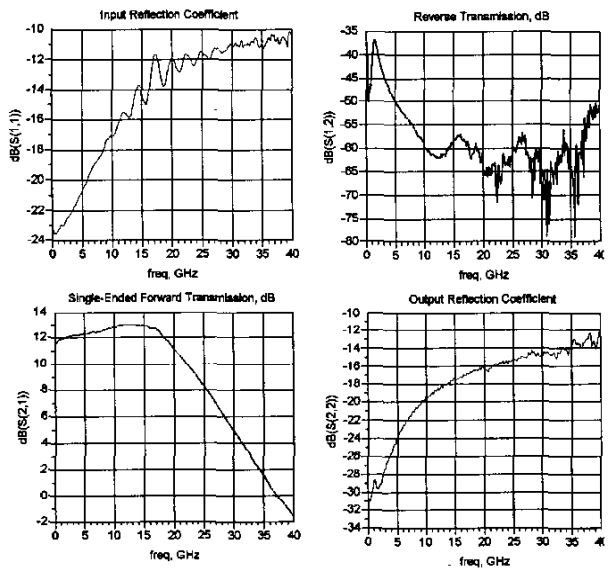

Fig. 6. S-Parameter measurement data at V_{DD}=1.2V.

V. Conclusions

In this paper we have demonstrated how broadband amplifiers can be built in advanced CMOS using monolithically integrated coupled inductors in a T-coil configuration. A bandwidth of 23GHz was achieved at a forward gain of 18dB, proving that CMOS will soon be commonplace in 40Gbit/s data transmission systems. To the authors' best knowledge, this is the highest bandwidth ever reported for an amplifier in CMOS technology.

ACKNOWLEDGEMENT

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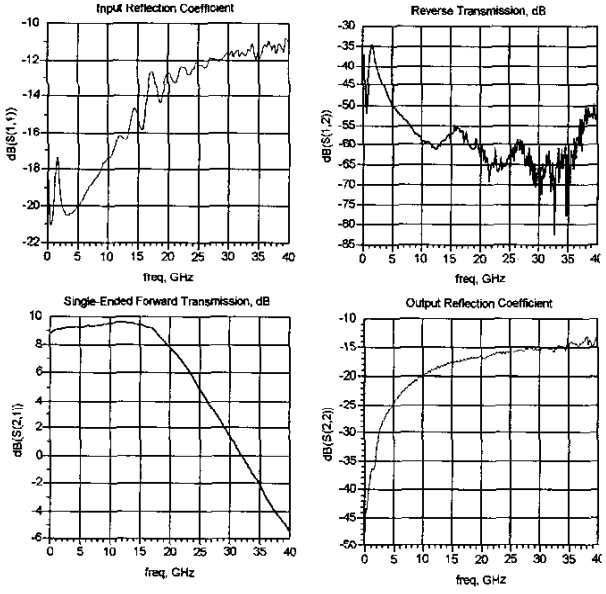

Fig. 7. S-Parameter measurement data at V_{DD}=1.0V.

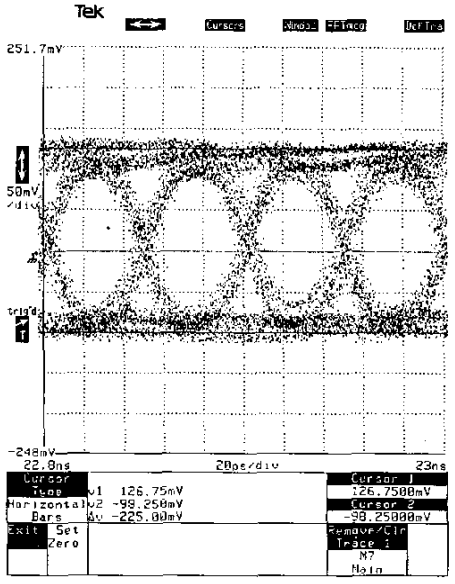

Fig. 8. Eye diagram at 20Gb/s.

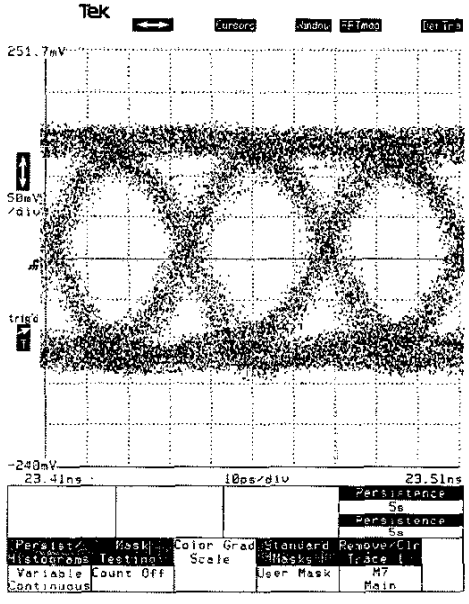

Fig. 9. Eye diagram at 30Gb/s.